## REMARKS[1]

In the outstanding Office Action, the Examiner rejected claims 1, 3 and 5-7 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,121,689 to Capote et al. ("Capote"), in view of U.S. Patent No. 6,426,556 to Lin ("Lin"); and rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Capote and Lin in view of U.S. Patent No. 6,077,726 to Mistry et al. ("Mistry").

By this amendment, Applicant has added new claims 21-24. Support for new claims 21-24 may be found in Applicant's specification at, for example, page 21, line 6 - page 24, line 27, and FIGS. 5 and 15. Claims 1, 3, and 5-24 are now pending in this application, with claims 1, 3, 5-8, and 21-24 currently presented for examination.

Applicant respectfully traverses the rejection of claims 1, 3, and 5-8 under 35 U.S.C. § 103(a) on the ground that the Examiner has not established a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicant declines to automatically subscribe to any statement of characterization in the Office Action.

requirements must "be found in the prior art, and not be based on applicant's disclosure." *See* MPEP § 2143, 8th Ed. (Rev. 4), October, 2005.

In this application, no *prima facie* case of obviousness has been established for at least the reasons that the references, in combination, fail to teach each and every element of the claims, and there is insufficient motivation for combining the references in the manner suggested by the Examiner.

A. Claims 1, 3, and 5-7

Claim 1 recites a combination including "a low dielectric constant insulating film having a relative dielectric constant of about 3.5 or less formed directly on a surface of the semiconductor chip." The Examiner concedes that "Capote does not teach a low dielectric constant insulating film formed on a surface of the semiconductor chip, and a passivation film formed on a surface of the low dielectric constant insulating film." Office Action, page 3.

To cure the above-noted deficiency of Capote, the Examiner cites Lin, stating

> Lin teaches a low dielectric constant insulating film on a semiconductor surface (Fig. 15, 29), and a passivation film formed on the insulating film (Fig. 15, 32) ... [and] [i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an insulating film and a passivation film on the chip surface of Capote as taught by Lin in order to provide surface protection for the chip. *Id.*

Contrary to the Examiner's assertion, Lin does not teach that dielectric layer 29 is a "low dielectric constant insulating film having a relative dielectric constant of about 3.5 or less formed directly on a surface of the semiconductor chip," as recited in amended

claim 1 (emphasis added). Lin only teaches a dielectric constant insulating film 29 formed on a semiconductor surface, and does not teach a low dielectric constant insulating film formed on a semiconductor surface. Lin does not define the dielectric constant insulating film 29 to be a low dielectric constant insulating film. Lin teaches only that "dielectric material for layer 29 can be used any of the typically applied dielectrics such as silicon dioxide (doped or undoped), silicon oxynitride, parylene or polymide, spin-on glass, plasma oxide or LPCVD oxide." Lin, column 7, lines 40-43. Not only does Lin fail to provide any teaching or suggestion that the listed materials have "a relative dielectric constant of about 3.5 or less," as recited in claim 1, but Applicant also respectfully submits that these materials do not have a relative dielectric constant of about 3.5 or less. Low K dielectric films typically include HSQ (Hydrogen Silsesquioxane), Organic Silica, porous HSQ, BCB (Benzocyclobutene), and the like (see Applicant's specification, at , for example, page 20, lines 5-9). Hence, the Examiner's assertion of "Lin teaches a low dielectric constant insulating film formed on a semiconductor surface (Fig. 15, 29)" is incorrect, and cannot be relied upon to cure the deficiencies of Capote. Accordingly, a *prima facie* case of obviousness has not been established.

Moreover, the Examiner states that "the passivation layer of Capote is being interpreted as the 'low dielectric constant insulating film' of claim 1," and that Lin "teaches a multilayer passivation layer, and in combining this feature with the Capote reference the passivation layer of Capote is 'low dielectric constant insulating film' of the

claim and the additional passivation layer taught by Lin is the 'passivation film' of the claim." Office Action, pages 4-5.

Even if this statement could be considered correct, Applicant submits that there is insufficient motivation for combining the cited references in the manner suggested by the Examiner. Capote, in FIG. 15, for example, teaches forming two bonding layers 32 and 34 on chip 10 wherein "chip bonding layer 32 is a thin polymer or coupling agent, with high adhesion to the chip passivation layer (not shown) on the face of the chip 10." Capote, col. 11, lines 29-32. Capote further teaches that chip bonding layer 32 is formed to "bond[] to the passivation layer on the chip 10 to provide high adhesive strength to the chip." Capote, col. 11, lines 40-41. Capote thus teaches that passivation layer is formed on the face of chip 10, and chip bonding layer 32 is formed over the passivation layer, such that there is high adhesion between the chip bonding layer 32 and the passivation layer, which provides a high adhesive strength to the chip 10.

According to the Examiner's proposed modification, however, an additional passivation film would be formed on the passivation film of Capote, and would essentially be formed between chip bonding layer 32 and the passivation layer of Capote. Thus, there would no longer be high adhesion between chip bonding layer 32 and the passivation layer of Capote, such that the chip 10 would no longer have high adhesive strength. Accordingly, not only do the cited references fail to provide sufficient motivation for the Examiner's proposed combination, they also teach away from such a

combination. Therefore, a *prima facie* case of obviousness has not been established for this reason also.

For at least the foregoing reasons, a *prima facie* case of obviousness has not been established with respect to claim 1. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claim 1 under 35 U.S.C. § 103(a).

Claims 3 and 5-7 depend from claim 1, and thus require all of the elements recited in claim 1. Because Capote and Lin fail to teach or suggest every element recited in claim 1, that combination of references also fails to teach or suggest every element required by dependent claims 3 and 5-7. Accordingly, a *prima facie* case of obviousness has not been established with respect to claims 3 and 5-7. Applicant therefore respectfully requests that the Examiner withdraw the rejection of claims 3 and 5-7 under 35 U.S.C. § 103(a).

B. Claim 8

Claim 8 depends from claim 1, and thus requires all of the elements recited in claim 1. As discussed above, Capote and Lin fails to teach at least "a low dielectric constant insulating film having a relative dielectric constant of about 3.5 or less formed directly on a surface of the semiconductor chip," as recited in amended claim 1, and required by claim 8. Mistry fails to cure this deficiency of Capote.

The Examiner appears to cite Mistry because the reference allegedly "teaches a passivation film comprising at least one layer formed of an organic film coating a connecting electrode (Fig. 1, 16)." Office Action, page 4. However, Mistry teaches "forming a polyimide layer (16) *over* a passivation layer (14)." Mistry, abstract

(emphasis added). Mistry thus fails to teach "a low dielectric constant insulating film having a relative dielectric constant of about 3.5 or less formed on a surface of the semiconductor chip," as recited in amended claim 1, and required by claim 8.

Since neither Capote, nor Lin, nor Mistry teaches or suggests every element required by claim 8, a *prima facie* case of obviousness has not been established. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claim 8 under 35 U.S.C. § 103(a).

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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Dated: October 30, 2006

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